MEMORY MODULE HAVING A PLURALITY OF INTEGRATED MEMORY COMPONENTS

The present invention relates to a memory module having a carrier substrate and a plurality of integrated memory components which are arranged on the carrier substrate.

For use in computer systems, for example, it is known, in order to form a memory module, to arrange a plurality of memory components, for instance, in the form of DRAMs (Dynamic Random Access Memories), on a common carrier substrate. Memory modules of this type are known, in particular, as DIMMs (Registered or Buffered Dual Inline Memory Modules). The latter are typically fit with 16 or 18 memory chips, which are clock-controlled when in the form of SDRAMs or DDR DRAMs.

Integrated memories, such as DRAMs, are operated in data processing systems and in this case are driven, for example, by a microprocessor or microcontroller. Above a certain size of the memory, for example, in the case of a memory size in excess of 1 Mbit, available DRAM memories generally use a multiplex address scheme. The latter primarily serves the purpose of reducing the number of address terminals of a memory and thus the costs for the individual components in the data processing system and the power consumption of the corresponding address bus systems.

A multiplex address scheme of this type has the advantage that it matches the functionality of a DRAM memory very well. For a memory access, firstly addressed rows in the form of selected word lines and then addressed columns in the form of selected bit lines are generally activated. In the case of this address scheme, firstly row addresses and, temporally thereafter, corresponding column addresses are thus

transmitted. A selection is thus made as to the memory cells from which data are read or the memory cells to which data are written. Together with address generation, a microcontroller likewise sends a plurality of individual commands, in particular, in the form of an activation signal, a read command or write command and, to conclude the memory access, a precharge command.

In order that a processor interface of a microprocessor and a DRAM interface can communicate with one another in a data processing system, for instance, a computer system, it is generally necessary to implement a memory controller (DRAM controller) in the computer system in order to convert the DRAM-specific memory access from the commands of the microprocessor. In this case, the memory controller is responsible, in particular, for mapping a logical processor address to the DRAM memory addressed and for generating the row addresses and column addresses for accessing the memory. For the purpose of realizing this functionality, registers and switching mechanisms (automatic state machines), which are suitable for this purpose, must be provided in the memory controller in order to realize this temporal multiplex address scheme. The provision of registers and switching mechanisms of this type increases the design complexity of a memory controller.

The present invention is based on the object of specifying a memory module of the type mentioned initially, which makes it possible, in the case of use in a data processing system, to reduce the design complexity of a memory controller to be provided in the data processing system.

This object is achieved according to the invention by means of a memory module in accordance with patent claim 1.

The memory module according to the invention includes a carrier substrate (having terminals for supplying address and command signals) and a plurality of integrated memory components, which are arranged on the carrier substrate. Provision is furthermore made of an access control circuit, which is arranged separately from the memory components on the carrier substrate and is connected, on the input side, to the terminals for supplying the address and command signals and, on the output side, to the plurality of integrated memory components. The access control circuit is designed in such a manner that, when supplying an address signal which has been generated outside the memory module, it receives an address for the memory access to a memory component which has been selected for the access. The access control circuit respectively generates, from the address received, at least one column address and row address for the purpose of accessing a bit line and word line of the selected memory component and transmits the column address and row address to the latter.

This means that there is, on the memory module according to the invention, an access control circuit, which undertakes the realization of the multiplex address scheme (for the purpose of accessing a memory of the memory module) on behalf of a memory controller and thus relieves the latter of this task. It is therefore no longer necessary to provide appropriate registers and switching mechanisms in the memory controller for the purpose of realizing the multiplex address scheme, with the result that the design complexity of the memory controller can accordingly be reduced.

In one development of the invention, the access control circuit is furthermore designed such that, when supplying an access command which has been generated outside the memory module and indicates the beginning of a memory access, it receives

the command and generates therefrom an access signal sequence for transmission to the selected memory component. The access signal sequence includes at least one activation signal and a subsequent read or write signal. This makes it possible for the memory module to receive only one access command from the memory controller, for example, whereupon the access control circuit generates, within the memory module, an activation signal followed by a read command or write command. This makes possible the need to transmit only one access command between the memory module and a connected memory controller for a memory access. The effective bandwidth of a command bus between the memory module and memory controller is thereby advantageously doubled.

In one advantageous embodiment of the memory module according to the invention, the access control circuit is arranged within a separate semiconductor module on the carrier substrate. In a further embodiment, the memory module is in the form of a DIMM module arrangement and the memory components are, in particular, in the form of dynamic random access memories.

Further advantageous designs and developments of the invention are specified in subclaims.

The invention is explained in more detail below with reference to the figures which are illustrated in the drawing, in which:

FIG. 1 shows an embodiment of a memory module in accordance with the invention, and

FIG. 2 shows an embodiment of a computer system having a memory controller and a plurality of memory modules in accordance with the invention.

FIG. 1 illustrates, in a roughly diagrammatic manner, an embodiment of a memory module in accordance with the invention. The present embodiment is a DIMM module arrangement, in the case of which a plurality of integrated memory components, in this case, in the form of DRAM memories 10 to 18 and 20 to 28, are arranged on a carrier substrate 50. An access control circuit 30, which is connected to a command and address bus CA and also to a clock signal line CK, is arranged separately from the memory components 10 to 18 and 20 to 28 on the carrier substrate 50. The input-side terminal of the access control circuit 30 is connected to the contact strip 40 of the memory module 1. The contact strip has terminals for inputting and outputting data signals DA, terminals for inputting a clock signal CLK and terminals for inputting address signals ADR and command signals CMD. On the input side, the access control circuit 30 is connected to the respective terminals of the contact strip 40 for supplying the address signals ADR and command signals CMD. On the output side, the access control circuit 30 is connected to a command and address bus CA1 for the first memory rank having the memories 10 to 18 and also to a command and address bus CA2 for the second memory rank having the memories 20 to 28. On the output side, the access control circuit 30 is furthermore connected to the clock signal line CK1 for driving the memories 10 to 18 of the first memory rank and to the clock signal line CK2 for driving the second memory rank having the memories 20 to 28. For the purpose of interchanging data, the memories 10 to 18 and 20 to 28 have respective data terminals DQ10 to DQ18 and DQ20 to DQ28 which may be connected to the data terminals DQ of the memory module 1.

As illustrated in more detail by the memory 10, by way of example, the individual memory components have memory cell arrays having word lines WL for selecting

memory cells MC and bit lines BL for reading data signals from, or writing data signals to, the memory cells MC. The memory cells MC are arranged in a known manner at crossover points of the word lines WL and bit lines BL and are respectively connected to one of the word lines and one of the bit lines. The memory cells MC each have a selection transistor and storage capacitor (not illustrated). The control input of the transistors being connected to a word line WL which activates connected memory cells MC in the event of a memory access.

The access control circuit 30 is designed such that, when supplying an address signal ADR which has been generated outside the memory module 1, it receives an address for a memory access to a selected memory component. The access control circuit respectively generates, from the address ADR received, at least one column address CADR for accessing a bit line BL and row address RADR for accessing a word line WL of the selected memory component, the column address CADR, and row address RADR being transmitted to the selected memory component via the command and address bus CA1, CA2. The access control circuit 30 furthermore receives an access command R/W which has been generated outside the memory module 1 (also see FIG. 2 in this respect). This access command indicates the beginning of a memory access. Once this access command has been received, the access control circuit 30 generates therefrom an access signal sequence having an activation signal ACT and, depending on whether a read or write access is involved, a subsequent read or write command RD or WR for transmission to the selected memory component. One command R/W is therefore required for a read or write access, with the result that the effective bandwidth of the command and address bus CA is doubled.

In accordance with the multiplex address scheme for a DRAM memory, the column address CADR and row address RADR for accessing a bit line and word line of a selected memory component are generated successively in time by the access control circuit 30 for transmission to the selected memory component. In particular, the column address CADR and row address RADR are generated such that they are offset by an RAS-CAS delay time tRCD defined by the type of selected memory component.

FIG. 2 diagrammatically illustrates an embodiment of an exemplary computer system having a memory controller 4 and a plurality of memory modules 1 and 2 constructed in accordance with the invention. The memory controller 4 is connected to a transmission bus 5. Both being situated on a so-called motherboard 3 of the computer system. The DIMM modules 1 and 2 are connected to the transmission bus 5 via plug connectors. The clock signal CLK, address signals ADR, command signals CMD, data signals DA and the access command R/W are transmitted to the DIMM modules 1 and 2 on the transmission bus 5.

For a memory access, only the access command R/W, i.e., either a read or write command, is transmitted, together with the full address ADR (n bits), from the memory controller 4 to the modules 1 and 2. The respective access control circuit 30 on the modules 1, 2 undertakes the DRAM-specific address multiplexing. This means that a row address RADR (r bits), together with an activation signal ACT, and subsequently a column address CADR (c bits), together with a read or write command RD, WR, are generated and transmitted to the selected memory component. In this case, $n = r + c$, it generally being the case that $r > n/2 > c$. The resulting unburdening of the memory controller 4 makes it possible to reduce the design complexity of the latter. In addition,

the access control circuit 30 advantageously enables decoupling between the transmission bus 5 of the motherboard 3 and the communication buses within the module. This makes it possible, for example, to operate the transmission bus 5 between the memory controller and DIMM modules at a higher data rate than the communication buses within the module.

List of reference symbols

1, 2	Memory module
3	Motherboard
4	Memory controller
5	Transmission bus
10 – 18	Memory component
20 – 28	Memory component
30	Access control circuit
40	Contact strip
50	Carrier substrate
CLK	Clock signal
ADR	Address signal
CMD	Command signal
DA	Data signal
CK, CK1, CK2	Clock signal line
CA, CA1, CA2	Command and address bus
DQ10 – DQ18	Data terminal
DQ20 – DQ28	Data terminal
DQ	Data terminals
RADR	Row address
CADR	Column address
ACT	Activation signal
RD	Read command
WR	Write command
MC	Memory cells
WL	Word lines
BL	Bit lines